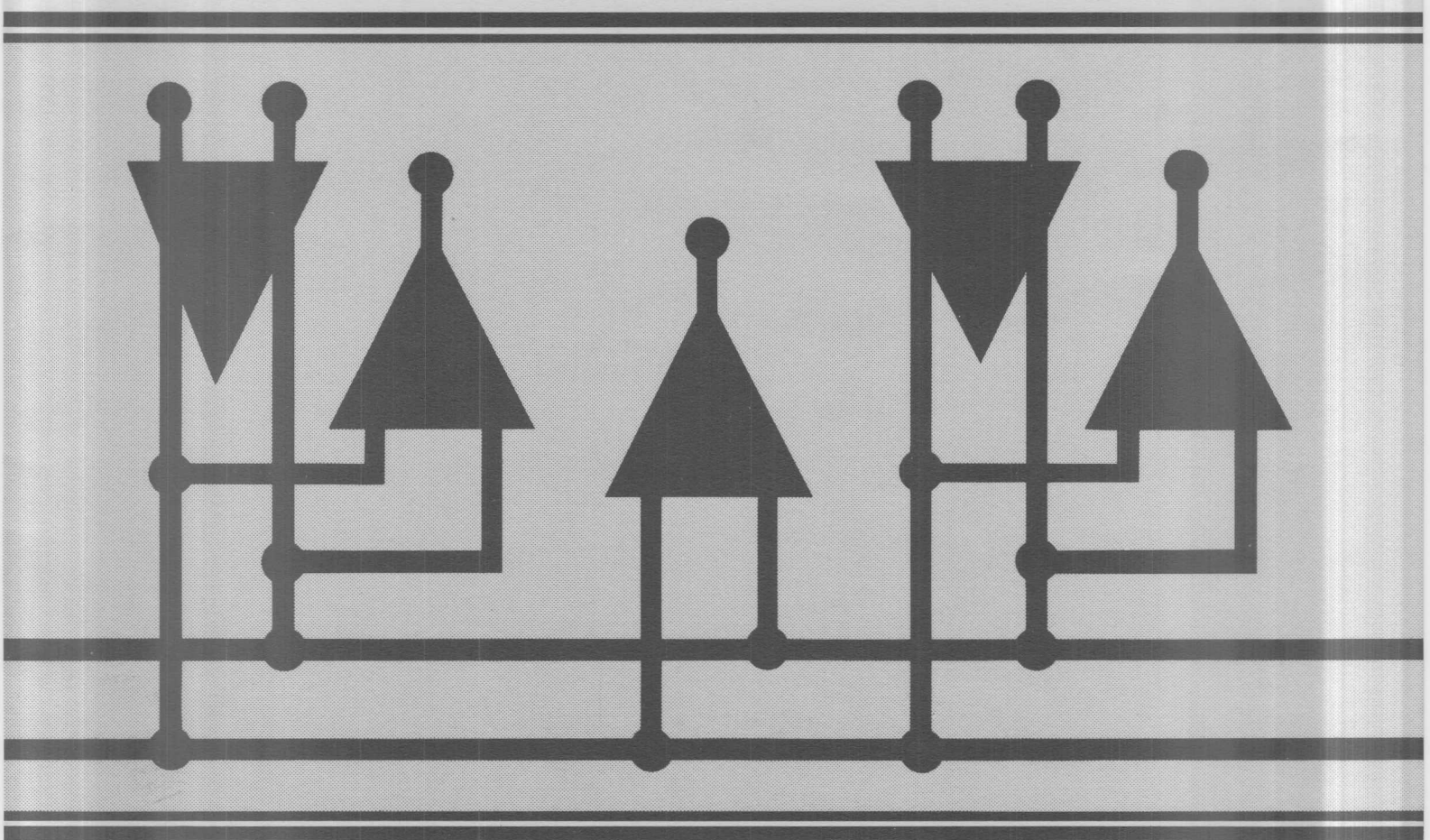
DATA COMMUNICATION

WITH LINEAR IC'S



AN006E

MOTOROLA Semiconductors

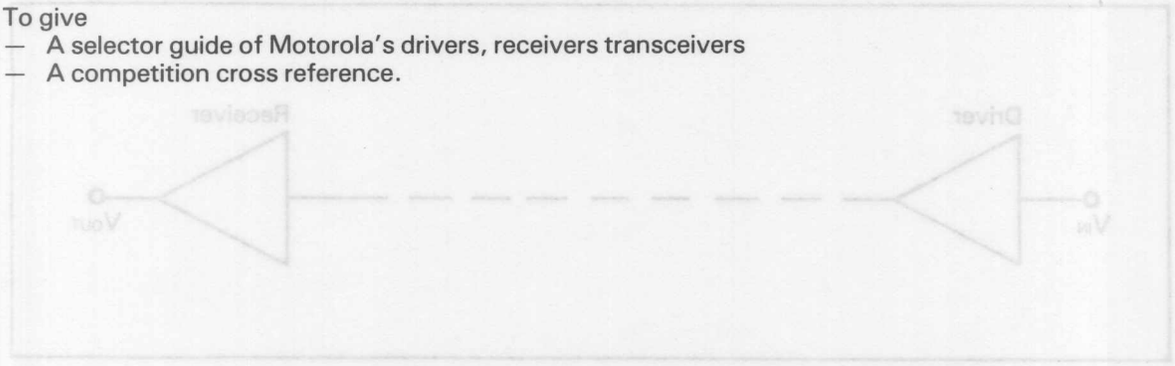
Introduction

The diversity of data communication systems has generated the need of many new interface integrated circuits.

Moreover, this need to interconnect individual pieces of equipment into complex systems has led to the establishment of several Interface standards to ensure equipment compatibility.

The purpose of this brochure is:

- To describe
  - The transmission systems
  - The characteristics of the Interface different standards
- To give
  - A selector guide of Motorola's drivers, receivers transceivers
  - A competition cross reference.



2. Line Driver

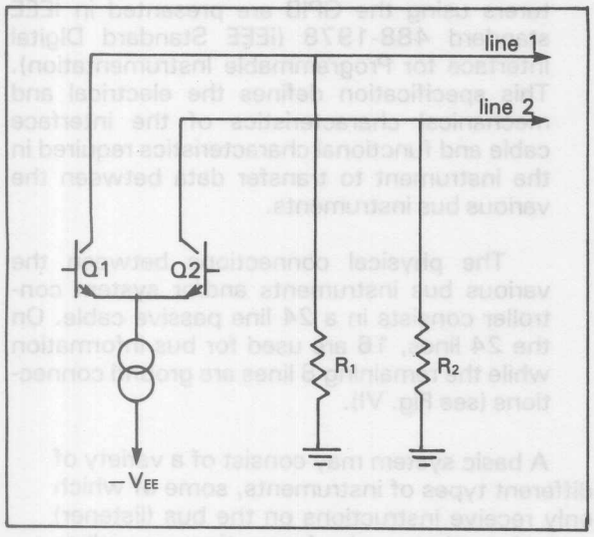


Fig. III — Differential open collector

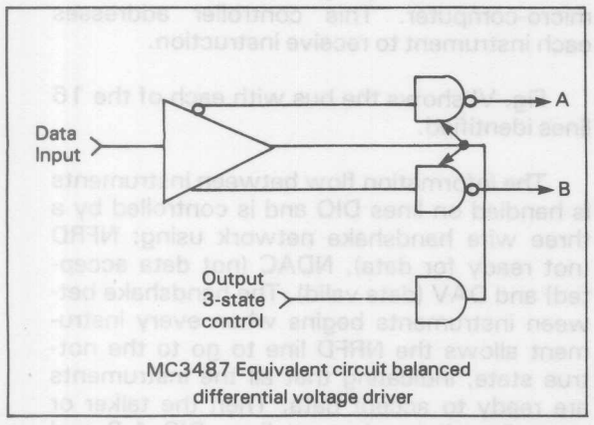


Fig. IV — MC3487 equivalent circuit balanced differential voltage driver

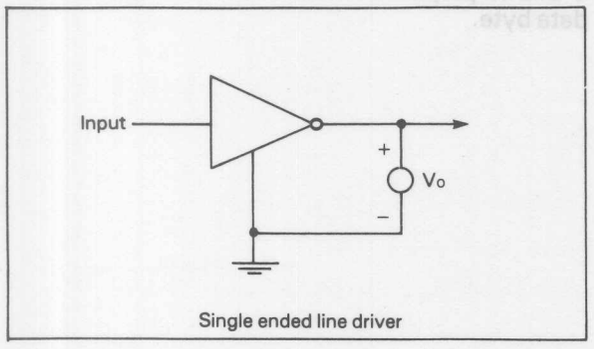


Fig. V — Single ended line driver

The Line driver purpose is to translate the input logic level (DTL, TTL, CMOS, etc.) to a signal more suitable for driving the line. An important exception to this is found in the MECL logic family, where MECL gates may be used to drive the line directly.

A popular method of driving lines between TTL systems is the differential open collector approach (Fig III).

A differential voltage, which is a function of the line terminations is created on the line.

Always one line is at ground potential line 1 goes low when Q1 conducts and line 2 remains at ground potential. Line 2 goes low when Q2 conducts and line 1 remains at ground potential.

An example of an IC driver using this technique is the MC75S110.

Other types of drivers include balanced differential voltage drivers (Fig IV) such as the MC3487.

In this type of circuit, the outputs are switched so that for a logic 1 input, output A > output B; for a logic 0 input, output B > output A.

The third type of driver is the single-ended voltage driver. The output of this type of driver is either positive or negative, with respect to the driver's ground, depending on the input. Fig V shows this type of driver.

Example of this type of driving: MC1488 or MC3488.

The remaining five lines are used for general bus control:

ATN (attention)	is used to specify if data on DIO lines are interface messages (addressing, etc.) or Instrument messages (DVM range, etc.).
IFC (Interface clear)	places the interface system into a known quiescent state.
REN (remote enable)	is used to select between local or remote control of the instrument.
SRQ (service request)	Is used by an instrument to indicate the need for attention and to request interruption of the current sequence of events.
EIO (end or identify)	is used to indicate the end of a multiple byte transfer sequence.

b) Bus transceivers

Fig. VII shows a block diagram of a GPIB compatible instrument.

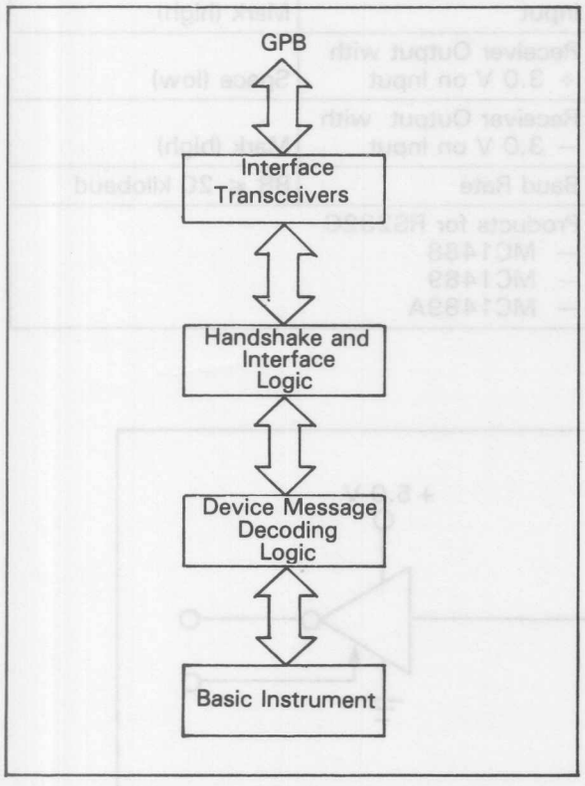


Fig. VII — GPIB compatible instrument

The interface transceivers provide coupling between the instrument logic levels (TTL, CMOS, etc.) and the standardized bus voltage levels. In addition, they provide receiver hysteresis for noise immunity.

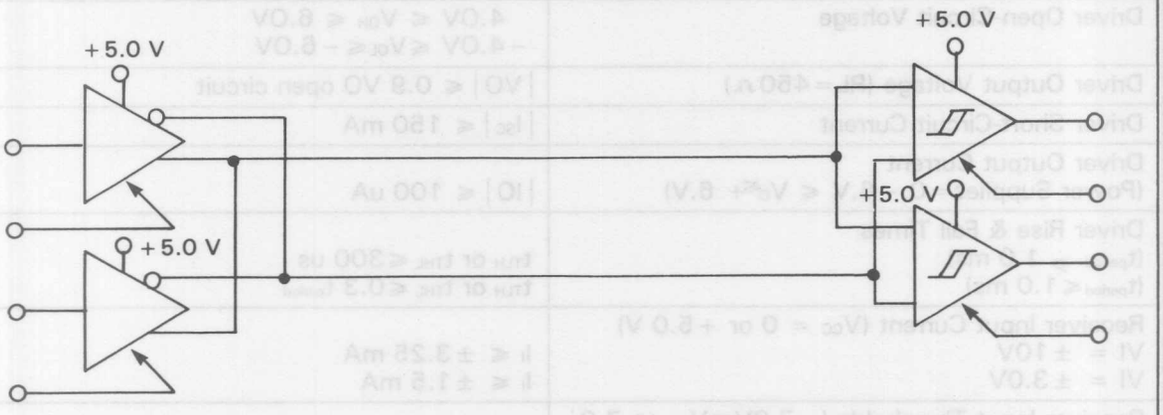
Integrated circuit implementation of these transceivers are provided by Motorola's MC3440, 41, 43, 46, 47, 48. All are quad interface transceivers (except MC 3447 which is octal) designed for interfacing between the GPIB and the instrument logic levels.

Four packages of transceivers — two packages with MC3447 — are required for a complete GPIB instrument interface, with each package providing four open collector drivers and four receivers with inputs hysteresis.

The input hysteresis provides increased signal line noise immunity.

2. RS422 data Communications

A high performance specification for data rates up to 10 megabaud, the RS422 standard employs a differential voltage mode configuration. The differential approach facilitates design of receiver structures that will reject noise which is common to both lines while detecting small differential signals. Ground path potential difference problems are also effectively suppressed. In addition, the complementary differential driver outputs permit to double the effective logic swing when operating on a single + 5 V supply.



Three State Drivers allow party line operation
(only one may be enabled at a time)

EIA RS422	
Driver Open-Circuit Voltage Differential Single Ended	$\lvert V_{OD} \rvert \leq 6.0$ V $\lvert V_O \rvert \leq 6.0$ V
Driver Output Voltage R_L = 50 Ω to Gnd (Each Output)	2.0 V $\leq \lvert V_{OD} \rvert \geq$ 0.5 V_{OD} (Open Circuit) $\lvert V_{OD} \rvert - \lvert V_{OD} \rvert \leq$ 0.4 V
Voltage from Junction of 50 Ω Resistors tied to Outputs to Gnd	$\lvert V_{OS} \rvert - \lvert V_{OS} \rvert \leq$ 0.4 V
Driver Short-Circuit Current	$\lvert I_{SC} \rvert \leq$ 150 mA
Driver Output Leakage Current (V_{CC} = 0, −0.25 V < V_O < + 6.0 V)	$\lvert i_O \rvert \leq$ 100 uA
DriverRise/Fall Times (10% + 90%) (Period of Output Pulse ≥ 200 ns (Period of Output Pulse ≤ 200 ns	 t_{TLH} or $t_{THL} \leq$ 0.1 Output Period t_{TLH} or $t_{THL} \leq$ 20 ns
Receiver Input Current (V_{CC} = On or off) V_I = ± 10 V V_I = ± 3.0 V	 $I_I \leq$ ± 3.25 mA $I_I \leq$ ± 1.50 mA
Receiver Input Thresholds (− 7.0 V ≤ $V_{CM} \leq$ + 7.0V)	$V_{TH} \leq$ ± 200 mV
Receiver Input Balance (V_I = ± 400 mV thru Balanced 500 Ω resistors, − 7.0 V ≤ $V_{CM} \leq$ + 7.0V)	 Receiver Maintains Correct Logic State Output
Baud Rate	BR ≤ 10 megabaud

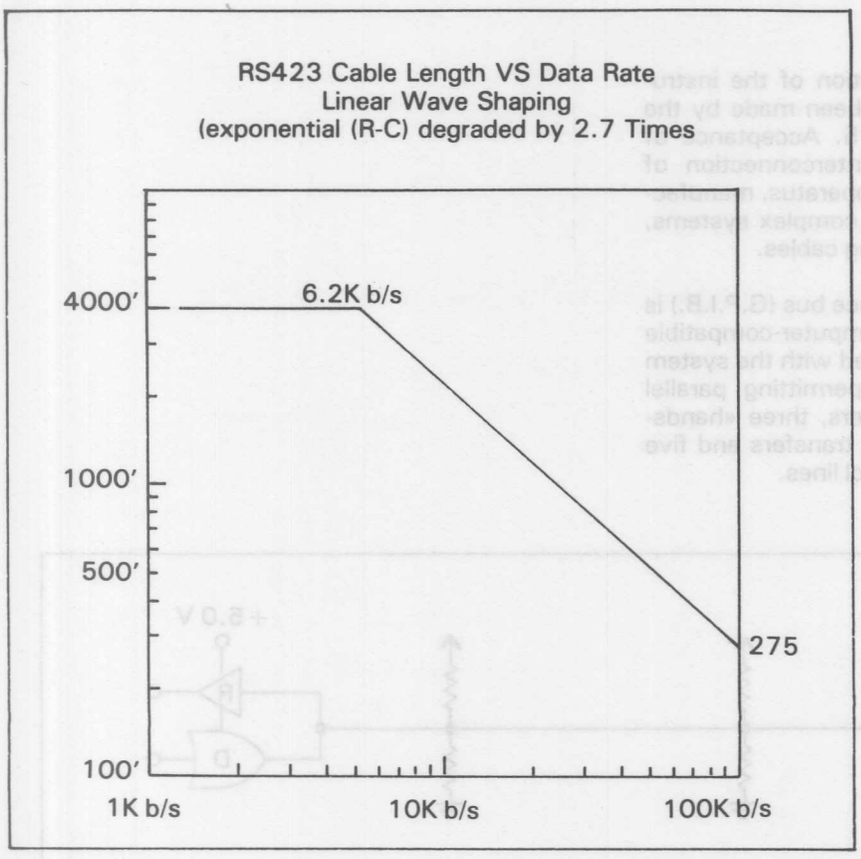
Products for RS 422
MC 3486
MC 3487
AM 26LS 31

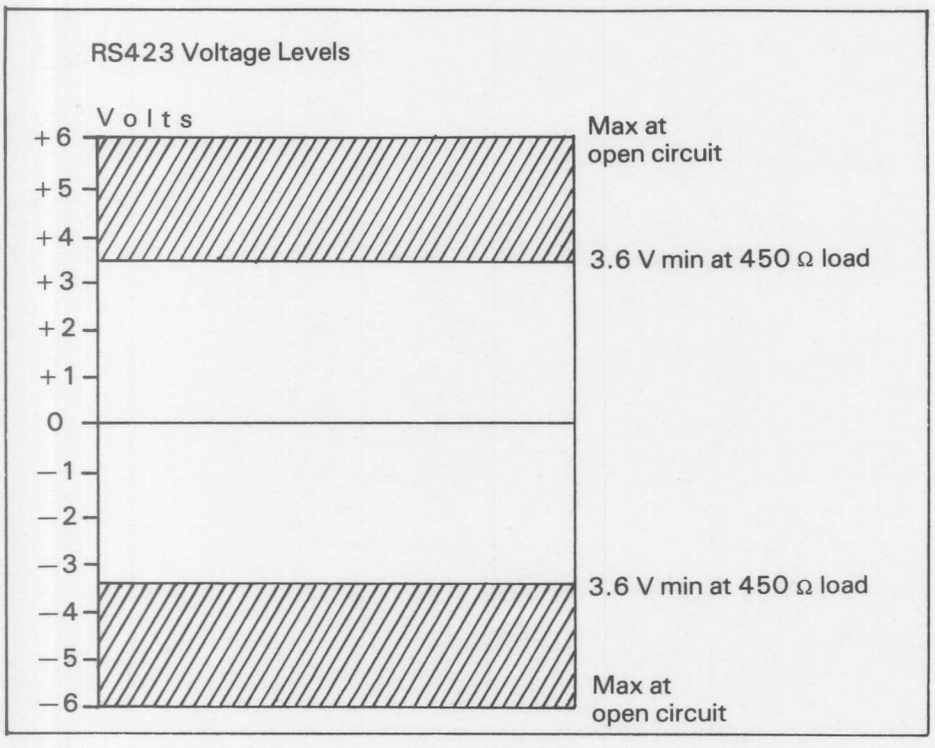
Comparison between the different standards

PARAMETER	RS232	RS422	RS423
Line Length (recommended max-may be exceeded with proper design)	50 ft	1200 m (4000 ft)	1200 m (4000 ft)
Input Z	3 to 7 kΩ	> 4 kΩ	> 4 kΩ
Max Frequency (baud)	20 kbaud	10 Mbaud	100 kbaud
Transition time* (time in undefined area between «1» and «0») tr = 10 to 90 %	4 % of r or 1 ms	tr ≤ 0.1 r r ≥ 200 ns tr ≤ 20 ns r< 200 ns	tr ≤ 3 r r < 1 ms tr ≤ 300 us r > 1 ms
dV/dt (wave shaping)	30V/µs	See transit. time	
Mark (Data «1») Space (Data «0»)	− 3 V + 3 V	A < B A > B	A = Negative B = Positive
Common mode Voltage (for balanced receiver)	—	− 7V < V_{CM} < 7V	—
Output Z	—	< 100 Ω balanced	< 50 Ω
Open circuit Output Voltage (V_o) V_t = loaded V_o	3V < |V_d| < 25V 5 < |V_d| < 15V 3 to 7.kΩ load	|V_d| < 6V** 2V or 5V_o < |V_t| 100 Ω bal.load	|V_t| ≤ .9|V_d| 450 Ω load
Short Circuit Current	500 mA	150 mA	150 mA
Power-Off Leakage (V_o applied to unpowered device)	> 300 Ω 2V < |V_d| < 25V V_o applied	< 100 µA 0 V < V_o < 6V V_o applied	< 100 µA |V_d| < 6V V_o applied
Min Receiver Input For Proper V_o	> ± 3 V	200 mV differential	> ± 3 V

* r is bit period

** across output, or output to ground


RS423 Cable Length VS Data Rate
Linear Wave Shaping
(exponential (R-C) degraded by 2.7 Times
4000'
1000'
500'
100'
6.2K b/s
275
1K b/s
10K b/s
100K b/s


RS423 Voltage Levels
Volts
+6
+5
+4
+3
+2
+1
0
−1
−2
−3
−4
−5
−6
Max at
open circuit
3.6 V min at 450 Ω load
3.6 V min at 450 Ω load
Max at
open circuit

IEE 488-1975	
Number of Devices	15 per system max
Number of Signal Lines	8 data, 8 control
Data Rate	1 Megabyte max
Transmission Path	20 meters total accumulated cable length max
Data Transfert	Byte-serial, bit-parallel, bidirectional using interlocked handshake technique
Driver Configuration	Open collector for SRQ, NRFD, NDAC Open collector or three-state for DIO 1.8, DAV, IFC, ATN, REN and EOI
Driver Output Voltage Low Logic State (I_{OL} = 48 mA) High Logic State Three-State (I_{OH} = −5.2 mA) Open collector (V_O = 5.25 V)	 $V_{OL} \leq 0.4$* 2.4 V min Leakage = 0.25 mA
Third State Leakage Current (V_O = 2.4 V)	± 40 µA max
Receiver Input Thresholds Low Logic State High Logic State	 ≤0.8 V ≥ 2.0 V
Receiver Thresholds (If Schmitt Trigger is Used) Low Logic State High Logic State Hysteresis	 + 1.1 V > V_{TH} − > 0.6 V + 2.0 V > V_{TH} + > 1.5 V ≥ 0.4 V
Resistive Termination Recommendations	3.0 k Ω to V_{CC} 6.2 k Ω to Gnd
Receiver Input Current Low Logic State (V_{IL} = 0.4 V) High Logic State (V_{IH} = 2.4 V) (V_{IH} = 5.25 V)	 − 1.6 mA max + 4.0 µA max + 1.0 mA max
DC Load Characteristics (I ≤ 0 mA) (I ≥ 0 mA) (I ≥ − 12 mA) (V ≤ 0.4 V) (V ≥ 0.4 V) (V ≤ 5.5 V) (V ≥ 5.0 V)	 V < 3.7 V V > 2.5 V V > − 1.5 V (if receiver present) I < 1.3 mA I > − 3.2 mA I < 2.5 mA I > 0.7 mA or small-signal Z must be ≤ 2.7 k at 1 MHz

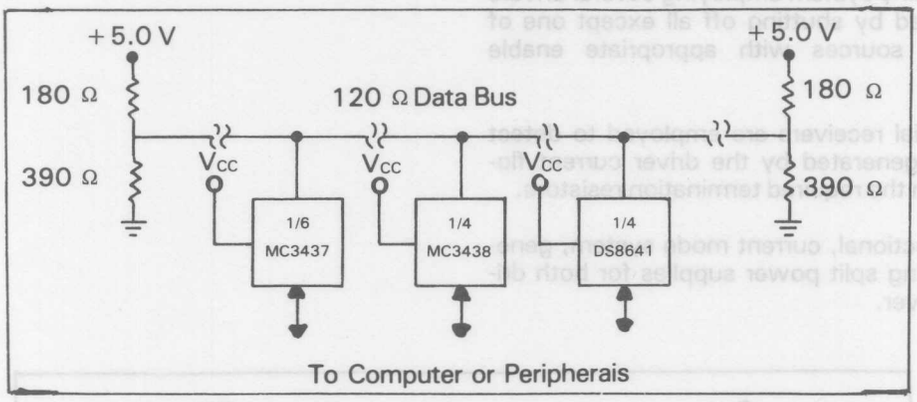
* May be changed to 0.5 V to permit Schottky devices

Products for IEEE 488-1975
- MC3440A
- MC3441A
- MC3443
- MC3446A
- MC3447
- MC3448A

6. Minicomputer

The unified bus system is widely employed for data I/O on popular minicomputer. It utilizes a single wire bidirectional voltage-mode system. Terminations are required on the lines.

The recommended drivers are open collector types and the receivers are available with or without hysteresis. Receiver outputs are active pull-up and input are fixed-reference differential amplifier types for low input loading.



UNIFIED BUS	
Termination	180 Ω to V_{CC} 390 Ω to Gnd
Impedance	120 Ω
Receiver Input Current (V_{IH} = 4.0 V, V_{CC} = 5.25 V	50 μA max
Receiver Input Threshold High State Low State Not Hysteresis Equipped High State Low State	 1.8 V ≤ V_{TH} + ≤ 2.5 V 1.05 V ≤ V_{TH} − ≤ 1.55 V 1.7 V min 1.3 V max
Bus Voltage - Low Logic State (Bus = 50 mA)	0.7 V max
Bus Current (V_{Bus} = 4.0 V, V_{cc} = 5.25 V or DV)	100 μA max
Driver Type	Open collector
Receiver Type	Differential amplifier, fixed reference

Products for Unified bus
- MC3437
- MC3438
- DS8641

	Device	Output current Capability	Prop. Delay Time	Single or Diff.	Party Line Operat.	Strobe or Enable	Power Supply	Logic Compati-bility	Corresponding receiver	Additional Features
DUAL	MC8T13L/P	75mA (min)	20	S	Yes	—	5 V	TTL/DTL	MC8T14	Outputs short circuit protected
	MC8T23L/P	59.3 mA (min)	20	S	Yes	—	5 V	TTL/DTL	MC8T24	
	MC3488L/P	150 mA	—	S	—	—	from ±9V to +15V	TTL/DTL	MC3486	RS423 and RS232C
	MC75S110L/P	12 mA	15 ns	Diff.	Yes	S	±5 V	TTL	MC75107 Mc 75108	TTL input compatiblity Schottky processing Inhibitor available for driver selection
	MC1488L/P	10 mA	175 ns	S	—	—	± 15 V	TTL/DTL	MC1489,A	Power-off source impedance 300 Ω min RS232C Simple slew rate control with external capacitor
	MC3453L/P	12 mA	15 ns	Diff.	Yes	S	±5 V	TTL	MC3450	Four independent drivers −3 V output common mode voltage over active operating range
QUAD	MC3487L/P	48 mA	15	Diff.	—	E	+ 5 V	TTL/DTL	MC3486	Schottky process RS422 Three state outputs
	MC3481L/P MC3485L/P	59.3 mA	25	S	Yes	E	+5 V	TTL	MC75125/7 MC75128/9	Compliance with IBM 360 370 Schottky processing. Separate enable and fault flag 3481. Common enable and fault flag 3485
	AM26LS31DC/PC	150 mA	20	Diff.	—	E	+ 5 V	Mos	AM26LS32	RS422 Spec Schottky processing Mos compatible

	Device	Single or	Type of output	Prop. Delay time (ms)	Strobe or enable	Power Supply	Logic compatibility	Corresponding Driver	Additional features
DUAL	MC75107 L/P	D	Totem pole	25	S	±5V	TTL/DTL	MC75S110	Input sensitivity ± 25mV Differential input common-mode voltage range of ± 30 V TTL or DTL drive capability
	MC75108 L/P	D	Open collector	25	S	±5 V	TTL/DTL	MC75S110	
TRIPLE	MC8T14 L/P	S	Totem pole	30	S	+5V	TTL/DTL	MC8T13	Each channel can be independently strobed Fully compatible TTL/DTL Input hysteresis results in high noise immunity Meet IBM 360/370 Spec
	MC8T24 L/P	S	Totem pole	30	S	+5 V	TTL/DTL	MC8T23	
QUAD	MC1489/A L/P	S	Common emitter	50	—	+ 5 V	TTL/DTL	MC1488	Meet EIA Standard RS232C Receiver performance identical to the MC75107/108 Four independent receivers Implied «AND» capability with open collector outputs (3452)
	MC3450 L/P	D	Totem pole	25	S	± 5V	TTL	MC3453	
	MC3452 L/P	D	Open collector	25	S	±5 V	TTL	MC3452	
	MC3486 L/P	D	Totem pole	25	3 State control	+ 5 V	TTL/DTL	MC3437 MC3488	Meet RS422/423 specification Receiver output 74LS compatible Four independent drains Internal hysteresis
	AM26LS32 DC/PC	D	Totem pole	25	E	5 V	MOS/TTL	AM26LS31	Meet RS 422/423 Spec Three state drive, with choice of complementary output enables, for receiving directly onto a data bus
HEX	MC3437 L/P	S	Totem pole	30	E	+ 5 V	TTL	MC3438 DS8641	Useful in system employing 120 Ω terminated lines Receiver TTL compatible
OTHER	MC75125/7 L/P	S	Totem pole	25	S	5 V	TTL/DTL	MC3481/5	Meets IBM 360/370 I/O Spec Schottky clamped transistor
	MC75128/9 L/P	S	Totem pole	25	S	5 V	TTL/DTL	MC3481/5	

COMPETITION CROSS REFERENCE	
Competitor	*Motorola Direct replac.*
Texas Instruments	
AM26S10CJ	MC26S10L
AM26S10CN	MC26S10P
AM26S11CJ	MC26S11L
AM26S11CN	MC26S11P
AM26LS31DC	AM26LS31DC
AM26LS31PC	AM26LS31PC
AM26LS32DC	AM26LS32DC
AM26LS32PC	AM26LS32PC
MC3446J	MC3446AL
MC3446N	MC3446AP
MC3486J	MC3486L
MC3486N	MC3486P
MC3487J	MC3487L
MC3487N	MC3487P
SN75107AJ	MC75107L
SN75107AN	MC75107P
SN75108AJ	MC75108L
SN75108AN	MC75108P
SN75121J	MC8T13L
SN75121N	MC8T13P
SN75122J	MC8T14L
SN75123J	MC8T23L
SN75123N	MC8T23P
SN75124J	MC8T24L
SN75124N	MC8T24P
SN75125J	MC75125L
SN75125N	MC75125P
SN75126J	MC3481/5L*
SN75126N	MC3481/5P*
SN75127J	MC75127L
SN75127N	MC75127P
SN75128J	MC75128L
SN75128N	MC75128P
SN75129J	MC75129L
SN75129N	MC75129P
SN 75138N	MC3443P*
SN75160J/N	MC3447L/P*
SN75161J/N	MC3447L/P*
SN75188J	MC1488L
SN75188N	MC1488P
SN75189AJ	MC1489AL
SN75189J	MC1489L
SN75189AN	MC1489AP
SN75189N	MC1489P
N8T26AJ	MC8626AL
N8T26AN	MC8T26AP
µA9636CJG	MC3488AU
µA9636CP	MC3488AP1

COMPETITION CROSS REFERENCE	
Competitor	*Motorola Direct replac.*
AMD	
AM1488 XC	MC1488L
AM1489 APC	MC1489 AP
AM1489 PC	MC1489 P
AM1489 AXC	MC1489 AL
AM1489 XC	MC1489L
AM26S10 DC	MC26S10 L
AM26S10 PC	MC26S10 P
AM26S11 DC	MC26S11 L
AM26S11 PC	MC26S11 P
AM26LS31 DC	AM26LS31 DC
AM26LS31 PC	AM26LS31 PC
AM26LS32 DC	AM26LS32 DC
AM26LS32 PC	AM26LS32 PC
N8T26 AB	MC8T26AP
N8T26 AF	MC8T26 AL
N8T28 B	MC8T28 P
N8T28 F	MC8T28 L
MC3448 AP/AL	MC3448 AP/AL
Intel	
6605 J/N	MC3443 P*
8216	MC8T26 AL*
8226	MC8T28 L*
SG	
SG1488 J	MC1488 L
SG1489 J	MC1489 L
SG1489 AJ	MC1489 AL
Raytheon	
RC 1488 DC	MC1488 L
RC1489 ADC	MC1489 AL
RC1489 DC	MC1489 L
RC8T13 DD	MC8T13 L
RC8T13 MP	MC8T13 P
RC8T14 DD	MC8T14 L
RC8T14 MP	MC8T14 P
RC8T23 DD	MC8T23 L
RC8T23 MP	MC8T23 P
RC8T24 DD	MC8T24 L
RC8T24 MP	MC8T24 P
RC75107 AD	MC75107 L
RC75107 ADP	MC75107 P
RC75108 AD	MC75108 L
RC75108 ADP	MC75108 P
RC75110 D	MC75S110 L
RC75110 DP	MC75S110 P
Signetics	
N8T13 F	MC8T13 L
N8T13 N	MC8T13 P
N8T14 F	MC8T14 L
N8T14 N	MC8T14 P
N8T23 F	MC8T23 L
N8T23 N	MC8T23 P
N8T26 AF	MC8T26 AL
N8T26 AN	MC8T26 AP
N8T28 F	MC8T28 L
N8T28 N	MC8T28 P